Atty. Docket No. OPP-GZ-2007-0009-US-00
Application No: 10/676,645

Remarks

Applicant and his representatives wish to thank Examiner Nadav for the thorough examination of the present application and the detailed explanations in the final Office Action dated October 15, 2007. Claim 1 has been amended to clarify the limitations regarding the alloy layer to obviate the rejection under 35 U.S.C. § 112, second paragraph. The Examiner's further concerns have been given serious consideration. However, the present claims are considered allowable over the cited references.

Claims 1, 4-5, 28, and 32 have been amended. Claim 38 has been added. Claims 1, 4-5, 8, 22-24, 27-32, and 34-38 are active in this application.

The present invention relates to a bonding pad of a semiconductor device comprising:

a) a via within an insulation layer over a metal line;

b) a barrier metal layer on a surface of the via;

c) a copper layer on the barrier metal layer within the via, the copper layer having vertical side surfaces that contact the barrier metal layer; and

d) an alloy layer on an upper surface of the copper layer within the via, the alloy having a top surface that is coplanar with or lower than a top surface of the insulation layer, wherein vertical side surfaces of the alloy layer contact the barrier metal layer, and the alloy layer consists essentially of copper and a low melting point metal selected from the group consisting of aluminum, lead, and silver (see Claim 1 above).

The cited references do not disclose or suggest, alone or taken together, a bonding pad including a copper layer in a via, an alloy layer on an upper surface of the copper layer, the alloy layer having vertical side surfaces that contact a barrier metal layer within the via, wherein the alloy layer consists essentially of copper and a low melting point metal selected from the group consisting of aluminum, lead, and silver (see steps c-d above). Thus, the present claims are patentable over the cited references.

The Rejections of Claims 1, 4-5, 8, 22-24, 27-32, and 34-37 under 35 U.S.C. § 112, Second Paragraph

The propriety of the rejections of the Claims as failing to point out and distinctly claim the invention in regard to the use of "consisting essentially of" in Claim 1 is respectfully traversed. The Examiner states that the use of "consisting" does not allow for the inclusion of additional elements and that the phrase "essentially of" indicates the inclusion of additional elements. However, the phrase "consisting essentially of" is a phrase that is an explicitly recognized in the MPEP for use in claim drafting. See M.P.E.P. § 2111.03; see also *In re Herz*, 537 F.2d 549, 551-52, 190 USPQ 461, 463 (CCPA 1976). (The transitional phrase "consisting essentially of" limits the scope of a claim to the specified materials or steps "and those that do not materially affect the basic and novel characteristic(s)" of the claimed invention.) Therefore, in view of the clear meaning of "consisting essentially of" as provided in the MPEP, the Examiner's rejection of the Claims based on the use of the phrase is not understood and is improper. As a result, this ground of rejection should be withdrawn.

The further bases of rejection under 35 U.S.C. § 112, second paragraph have been obviated by appropriate amendment.

Rejection of Claims 1, 4-5, 23-24, 27-32 and 34-37 under 35 U.S.C. § 102(e)

The rejection of Claims 1, 4-5, 23-24, 27-32 and 34-37 under 35 U.S.C. 102(e) as being anticipated by Matsubara (U.S. 6,890,852) is respectfully traversed.

Claim 1 of the present application may be exemplified by a bonding pad 200 comprising a copper layer 3 over a barrier metal layer 10 within a via 100, the copper layer 3 having vertical side surfaces that contact the barrier metal layer 10, an alloy layer 5 on an upper surface of the metal layer 3, the alloy layer 5 having vertical side surfaces that contact the barrier metal layer 10 within the via 100, wherein the alloy layer 5 consists essentially of copper and a low melting point metal selected from the group consisting of aluminum, lead, and silver (see, e.g., paragraphs [0011]-[0016], and FIG. 1F).

Matsubara discloses a method of forming a semiconductor device including forming a bump electrode 13 on a solder layer 12 (containing Pb or Sn) over a copper buried wiring 8 for use in a flip chip method (see, e.g., col. 5, l. 47-col. 6, l. 11, and FIG. 1). A bump is a structure that is known in the art of semiconductor manufacturing and is distinct from a bonding pad. Bumps are typically formed over bonding pads on a substrate (see, e.g., Wolf, Silicon Processing for the VLSI Era, Volume 1 – Process Technology [2nd ed. 2000], pp. 857-858, Section 17.5.4, first paragraph; submitted herewith). Specifically, Wolf teaches that solder bumps (typically containing Pb and Sn) are fabricated directly over bonding pads (e.g., Al bonding pads) in flip-chip technologies (see Wolf, *supra*, pp. 857-859, Section 17.5.4, first-third paragraphs and FIGS. 17-15 and 17-16(a)). Consistent with the understanding in the art, the present claimed bonding pad (see, e.g., bonding pad 200 in FIG. 1F of the present application) is distinct from the solder layer 12 (containing Pb or Sn) and the bump electrode 13 of Matsubara, which together appear to comprise a flip-chip bump structure as described by Wolf.

Therefore, it appears the only structures disclosed by Matsubara that may be compared with the bonding pad structures of the present Claims are the buried copper wirings. Matsubara discloses copper thick films 10 and 22, and a copper thin films 9 and 21 that are comprised within copper buried wirings 8 and 25, which may be made of pure copper or copper alloys (see, e.g., col. 6, ll. 37-43, col. 9, ll. 10-17, col. 10, ll. 20-22, and FIGS. 1 and 12). However, Matsubara does not disclose or suggest that copper thick film 10 and copper thin film 9 of copper buried wiring 8 are composed of different materials. Nor does Matsubara disclose or suggest that copper thick film 22 and copper thin film 21 of copper buried wiring 25 are composed of different materials. Rather, Matsubara discloses that "*the copper buried wiring*" (e.g., copper buried wirings 8 and 25, which include the thin and thick copper films 9 and 10, and 21 and 22, respectively) may alternatively be composed of copper-Al alloys, copper-Ag alloys, or copper-silicon alloys (see, e.g., col. 10, ll. 20-22, and FIGS. 1 and 12). Thus, Matsubara's description of the copper buried wiring structures 8 and 25 does not disclose an alloy layer on an upper surface of a copper layer in a via, wherein the alloy layer consists essentially of copper and a low melting point metal selected from the group consisting of aluminum, lead, and silver, as recited in Claim 1.

Also, amorphous film 29 over copper thick film 10 comprises copper and tantalum (see, e.g., col. 9, ll. 9-28 and FIG. 14), and thus does not represent an alloy layer consisting essentially of copper and a metal selected from the group consisting of Al, Pb, and Ag.

Furthermore, the vertical side surfaces of copper thick films 10 and 22 appear to contact only the thin metal films 9 and 21, respectively (see, e.g., FIGS. 1 and 12). The copper layer and the barrier metal layer of present Claim 1 cannot simultaneously read on the same structure (e.g., thin copper wiring 9 or 21). Therefore, it cannot be argued that the copper thick film (10 or 22) of Matsubara is an alloy layer that is on an upper surface of a copper layer (e.g., copper thin film 9 or 21), ***and*** that vertical side surfaces of the copper thick film (10 or 22) contact a barrier metal layer (e.g., thin copper wiring 9 or 21). Thus, Matsubara is deficient with regard to an alloy layer on an upper surface of a metal layer, the alloy layer having vertical side surfaces that contact a barrier metal layer within a via, as recited in Claim 1.

Therefore, Matsubara is deficient with regard to a bonding pad comprising a copper layer in a via, an alloy layer on an upper surface of the copper layer, the alloy layer having vertical side surfaces that contact a barrier metal layer within the via, wherein the alloy layer consists essentially of copper and a low melting point metal selected from the group consisting of aluminum, lead, and silver, as recited in Claim 1.

As a result of the deficiencies explained above, Matsubara does not anticipate the present Claim 1, and the rejection under 35 U.S.C. § 102(e) is not sustainable and should be withdrawn. Claims 4-5, 23-24, 27-32 and 34-37 depend from Claim 1 and thus include all of the limitations of Claim 1. Thus, Matsubara fails to anticipate Claims 4-5, 23-24, 27-32 and 34-37 for at least the same reasons as Claim 1.

Rejection of Claims 8 and 22 under 35 U.S.C. § 103(a)

The rejection of Claims 8 and 22 under 35 U.S.C. § 103(a) as being unpatentable over Matsubara in view of Liu et al. (US 6,638,867, hereinafter "Liu") is respectfully traversed.

As discussed above, Matsubara is deficient with regard to a bonding pad comprising a copper layer in a via, an alloy layer on an upper surface of the copper layer, the alloy layer having vertical side surfaces that contact a barrier metal layer within the via, wherein the alloy layer consists essentially of copper and a low melting point metal selected from the group consisting of aluminum, lead, and silver, as recited in Claim 1.

Liu discloses a bonding pad 60 that includes an aluminum alloy (alternatively copper) bonding pad segment 54 in a shallow interconnection line 40 (see col. 6, ll. 16-27, and FIGS. 6C-6D) and an aluminum conductive layer 58 over the bonding pad segment 54 (see col. 6, ll. 34-42, and FIG. 6C). Liu further discloses that the conductive layer 58 over the bonding pad segment 54 can alternatively consist of aluminum alloy, tungsten, copper, or a copper alloy (see col. 6, ll. 35-40). Liu does not appear to teach or disclose that the non-aluminum metal in the aluminum alloy alternative is copper, or that the non-copper metal in the copper alloy alternative is aluminum (see col. 6, ll. 34-40). Therefore, Liu fails to cure the deficiencies of Matsubara with regard to an alloy layer on an upper surface of a copper layer, the alloy layer consisting essentially of copper and a low melting point metal selected from the group consisting of aluminum, lead, and silver, as recited in Claim 1.

Additionally, Liu fails to disclose forming a barrier metal layer in shallow interconnect line 40 (see, e.g., col. 5, ll. 20-36, and FIGS. 5A-5B). Furthermore, conductive layer 58 is not formed within shallow interconnect line 40, and thus would not have vertical side surfaces in contact with a barrier metal layer even if Liu disclosed forming a barrier metal in shallow interconnect line 40 (see, e.g., col. 6, ll. 16-42, and FIG. 6A-6C). Thus, Liu fails to cure the deficiencies of Matsubara with regard to a bonding pad comprising a copper layer in a via, an alloy layer on an upper surface of the copper layer, the alloy layer having vertical side surfaces that contact a barrier metal layer within the via, wherein the alloy layer consists essentially of copper and a low melting point metal selected from the group consisting of aluminum, lead, and silver, as recited in Claim 1.

As a result, Liu fails to cure the deficiencies of Matsubara with regard to the device of Claim 1. Therefore, Claim 1 is patentable over Matsubara in view of Liu. Claims 8 and 22

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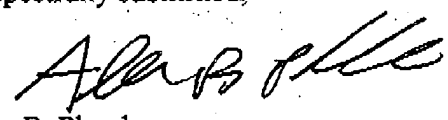
depend from Claim 1 and thus include all of the limitations of Claim 1. Thus, Claims 8 and 22 are patentable over Matsubara in view of Liu for at least the same reasons as Claim 1, and the rejection under 35 U.S.C. § 103(a) should be withdrawn.

Conclusions

In view of the above amendments and remarks, all bases for objection and rejection are overcome, and the application is in condition for allowance. Early notice to that effect is earnestly requested.

If it is deemed helpful or beneficial to the efficient prosecution of the present application, the Examiner is invited to contact Applicant's undersigned representative by telephone.

Respectfully submitted,



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PROCESS TECHNOLOGY

Second Edition

STANLEY WOLF Ph.D.

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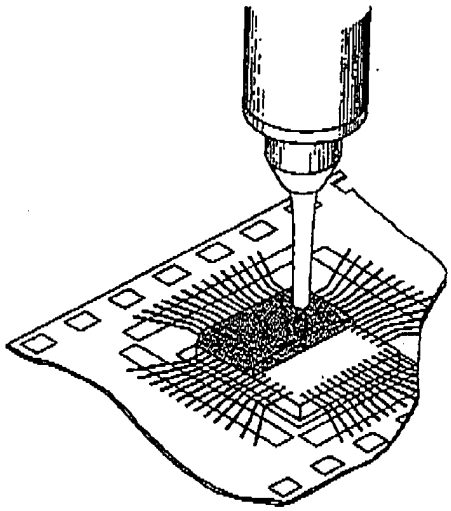

Fig. 17-13 TAB encapsulation.[2] Reprinted with permission of Van Nostrand Reinhold.

wire bonds) TAB also offers a lower profile, which makes TAB applicable for smart-cards, watches, read/write head circuitry, flash memory modules, and the like. The disadvantages of TAB are: 1) it requires a special tape design for each different chip design; 2) there is less infrastructure to provide testability of packaged TAB parts and for mounting the packaged TAB parts to the next levels of packaging; and 3) higher cost compared to wire bonding.

17.5.4 Flip-Chip Bonding

In *flip-chip technologies* solder bumps are fabricated directly on the Al bonding pads of the chip. The chip is then flipped face down and aligned to the package or substrate. The bumps are

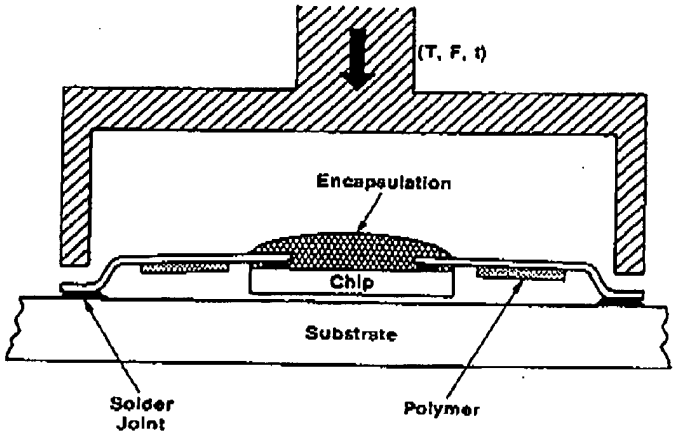

Fig. 17-14 TAB outer lead bonding.[2] Reprinted with permission of Van Nostrand Reinhold.

bonded directly (and all at once) to the package (or substrate) pads by reflowing the solder bumps. The process was introduced by IBM in 1964, and they called it C4 for *controlled collapse chip connection*.[14] The advantages of flip-chip bonding are: 1) the entire chip surface can be covered with solder bumps (making it an *area-array interconnect*). In other words, bonding locations are not limited to the chip perimeter, thus more I/O capability is provided than by a perimeter-interconnect on a die with the same size; and 2) the very short lengths of the chip-to-package interconnect paths minimizes their inductance.

As in TAB, the bumps are formed while the chip is still in wafer form. The bump formation process represents an added expense to overall wafer fabrication cost. However, since this process eliminates the cost of wire bonding, other production costs are reduced. Furthermore, the bump metallurgy reseals the area over the bonding pads that otherwise remains open after wire bonding. Thus, flip-chip technology hermetically seals the chip without the need for a package. This attribute is being exploited for so-called "packageless" attachment of die to substrates (discussed in Section 17.10.2).

The solder bumps most widely used to attach chips to alumina ceramic substrates have been high lead solders, especially 95 Pb:5 Sn. This solder melts at the relatively high temperature of 315°C, which permits other lower-melting-point solders to be used in subsequent module-to-card, or card-to-board packaging level processes without remelting the flip-chip bonds. A multi-layer film of metal (e.g., Cr-Cu-Au) is sandwiched between the Al chip pad and the solder bump to prevent the solder from interdiffusing into the Al. The Cr-Cu-Au film forms a cap over each of the Al bonding pads, and the size of each cap is also restricted by sequentially evaporating the Cr-Cu-Au film through a mask (Fig. 17-15a). The Pb:Sn is next evaporated onto the chip, again through a mask. The local area of each Pb:Sn layer is slightly larger than the area of the cap. Heating the wafer in an H_2 ambient at 350°C melts these localized Pb:Sn layers. The surface tension of the liquid solder causes the film to recede from the oxide surface, and to form a solder ball on top of the Cr-Cu-Au cap. The diameter of the base of these spherical bumps is determined by the dimension of the Cr-Cu-Au cap. This process is called *ball-limiting metallization* or BLM (see Fig. 17-16). Note that bumps made of conductive epoxy, which allow

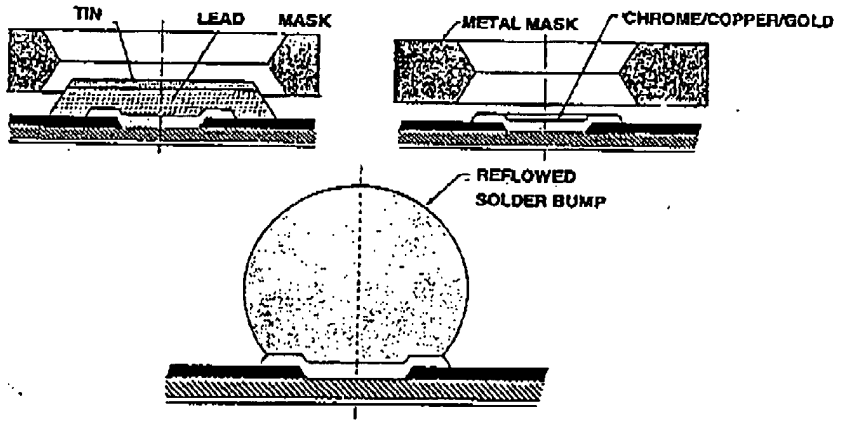

Fig. 17-15 Fabrication of solder bumps for C4 technology.[15] © ISHM 1974.

lower temperature processing than solder bumping, have been pioneered by the Polymer Flip-Chip Corp.[16,17]

Following the reflow of the solder bumps that connect the chip to the substrate, an underfill adhesive is formed between the chip and the substrate.[18] Such underfilling is necessary to reduce the stress on the solder bumps during temperature cycling. When the underfill adhesive is present, it shoulders a large fraction of the stress burden, and the stress on the bumps is significantly reduced. This decreases their tendency to fail through solder-bump stress fatigue.

The underfill adhesive (an epoxy or polyimide) is dispensed as a bead along the perimeter of the bump-attached chip. The chip is heated to 70–100°C and this lowers the viscosity of the underfill epoxy so that capillary force wicks it into the space underneath the die. Once flowed into place, the epoxy is cured to its solid form by an additional heat-curing step.

The term "flip chip" refers only to the method of attachment. No indication is made about what the chip is attached to. That is, if the chip is attached to a package it is called *flip-chip in package* (FCIP) and this method applies to single chip packages and multi-chip modules (MCMs). FCIP is used when the electrical performance of wire bonds is inadequate or when the number of I/Os is too large for wire bonding. Use of FCIP together with a ball-grid array package (see Sect. 17-10) would represent a packaged chip with a very large I/O count. For example, the Intel Pentium II microprocessor is put into plastic and ceramic BGAs and MCMs with flip-chip attach. *Direct chip attach* (DCA) refers to the direct attachment of a chip to a printed circuit board (also called *flip-chip on board*). *Flip-chip DCA* (FC-DCA) bypasses the attachment of the chip to the package.

Flip-chip attachment, however, has some limitations, including the following:

1. The infrastructure for manufacturing, testing, and handling flip-chips from semiconductor vendors by 1998 was not yet mature. Yet, forecasts were that by 2001 the number of chips requiring FC bumping will have increased to more than 2.5 billion. Furthermore, by 1998, flip-chip foundries were beginning to emerge.
2. A lack of standards exists for these procedures, due to the limited adoption of the flip-chip technology by the late 1990's.

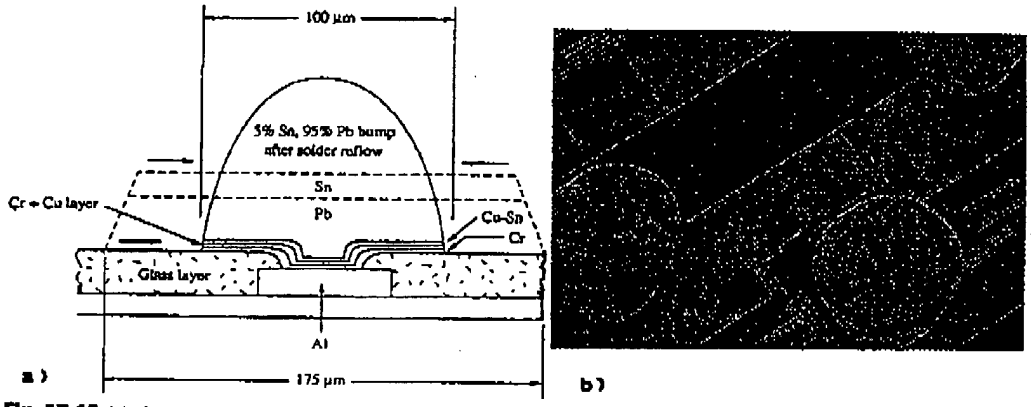

Fig. 17-15 (a) Cross section of a solder bump used in flip-chip technologies and the deformation caused by reflow-soldering operations; (b) SEM view of the C4 solder bumps on a chip.[14] Reprinted with permission of IBM Corporation.

3. Some of the manufacturing issues are also difficult. For example, visual verification of bump placement is not easy, making die placement accuracy very important. Thermal cycle fatigue of the solder joints is also a problem, especially if an underfill material is not used. The viscosity of the underfill epoxy material, however, changes with time, making the under-fill wicking process vary over the space of a day or shift. Another problem is that most ordinary Pb solders contain trace quantities of radioactive elements (i.e., which emit alpha particles that can cause soft errors in memory circuits). Solders made from lead that emits low levels of alpha particles are available for applications that cannot tolerate high soft error rates.

17.6 INTRODUCTION TO CHIP PACKAGES

Integrated circuit chips (or die) are usually encapsulated in an IC package prior to their being installed into electronic systems.[19] IC packages perform four key functions:

1. They provide a sturdy set of leads that allow an IC to be connected to the system in which it will operate. These leads, however, should not significantly degrade the performance of the chip housed by the package.
2. They provide physical protection for the chip against breakage or scratching.
3. They provide environmental protection for the chip against damage from chemicals, moisture, or gases.
4. They dissipate the heat generated by the chip during operation. Chips generating large quantities of heat require additional measures to be incorporated into the package design.

In order to achieve the above objectives, packages are designed to have the following characteristics: 1) low lead capacitance and inductance; 2) material compatibility; 3) good thermal conductivity; 4) good hermetic integrity; 5) ease of manufacture; 6) low cost; and 7) stress levels that will not harm the chip or package. ICs in packages are also easier to handle and test than bare die. They make it easier to compensate for the mismatches in coefficients of thermal expansion among the materials used in the construction of electronic systems. Chip packages, however, also impact the cost, reliability, and sometimes even the performance of the IC (and maybe even the system in which the IC is being used). Reduction in the prices of electronic systems have primarily been driven by the shrinkage of the IC devices themselves, but improvements in packaging have also helped decrease these costs. Packaging cost is important because it can account for a significant fraction of the total cost of the packaged IC. This cost, as measured by cost per pin, has increased from about 1 cent ($US) per pin in small-scale and medium-scale ICs (SSI and MSI), to about 10 cents per pin for ULSI. For ULSI devices in ceramic packages, the package cost may exceed the chip cost by more than 2 times.

In the upcoming sections IC packages will be described. The discussion begins by comparing hermetic (ceramic) and non-hermetic (plastic) packages. Then various IC package types (i.e., through-hole versus surface mount, and specific package configurations) will be analyzed. Finally, so-called "packageless" techniques for ICs are described.

IC package technology is generally divided into two categories, namely: *hermetic* and *non-hermetic* (i.e., plastic) packages. In hermetic packages the chip is housed in an environment isolated from the external world by a vacuum-tight enclosure. The package material is usually ceramic-based, and the two most widely used hermetic-package types are *ceramic packages* and *glass-sealed refractory (cerdip) packages*. Such packages are used in high-reliability